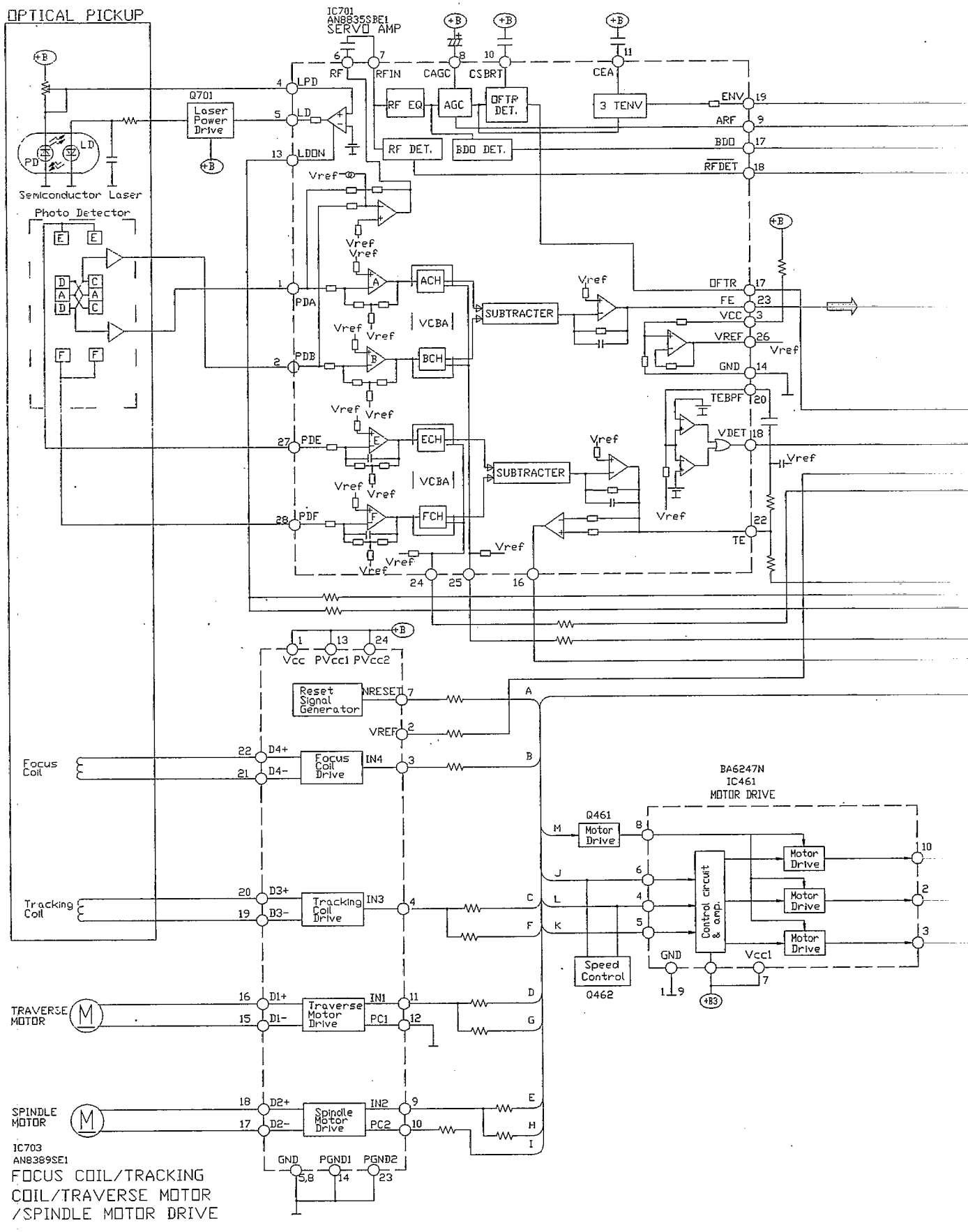
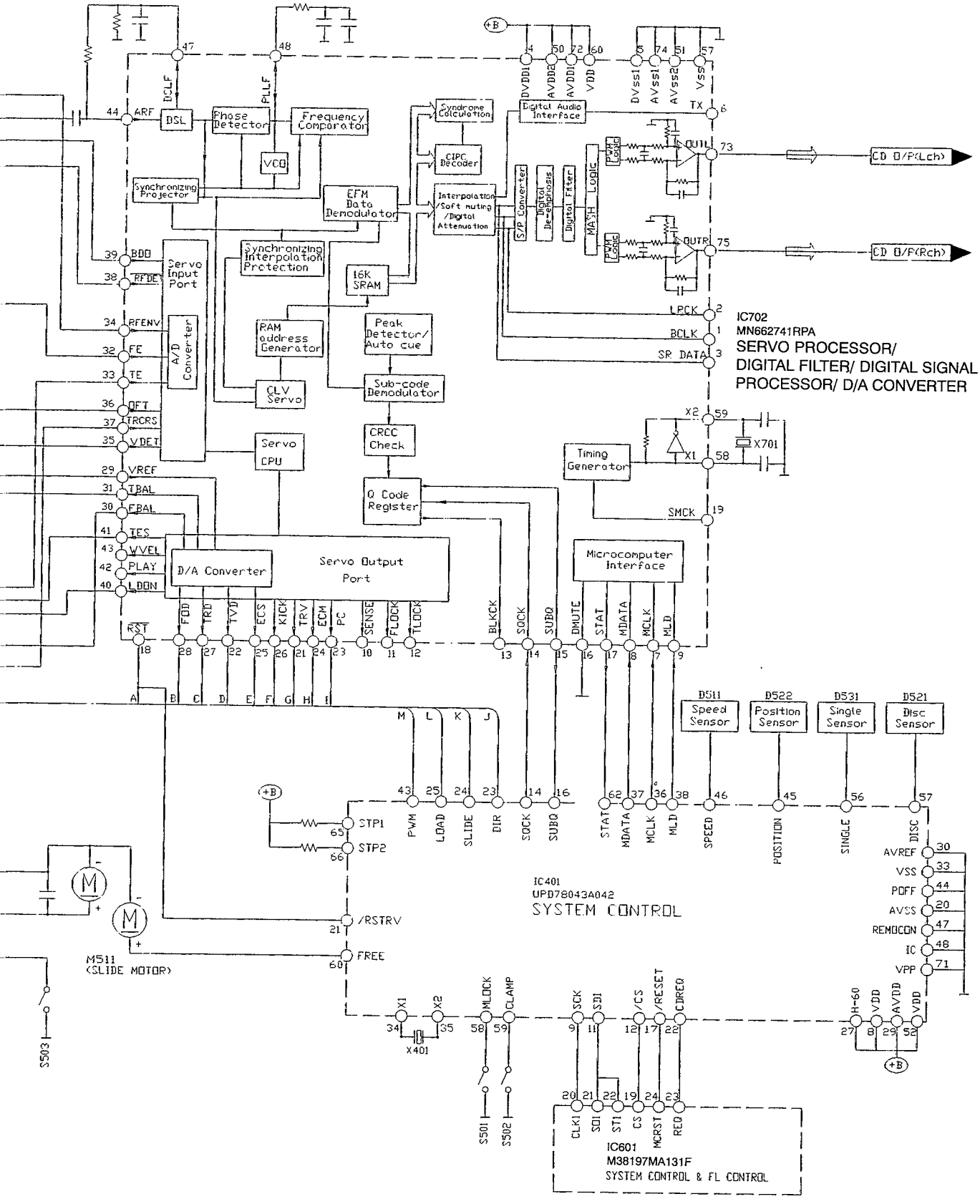
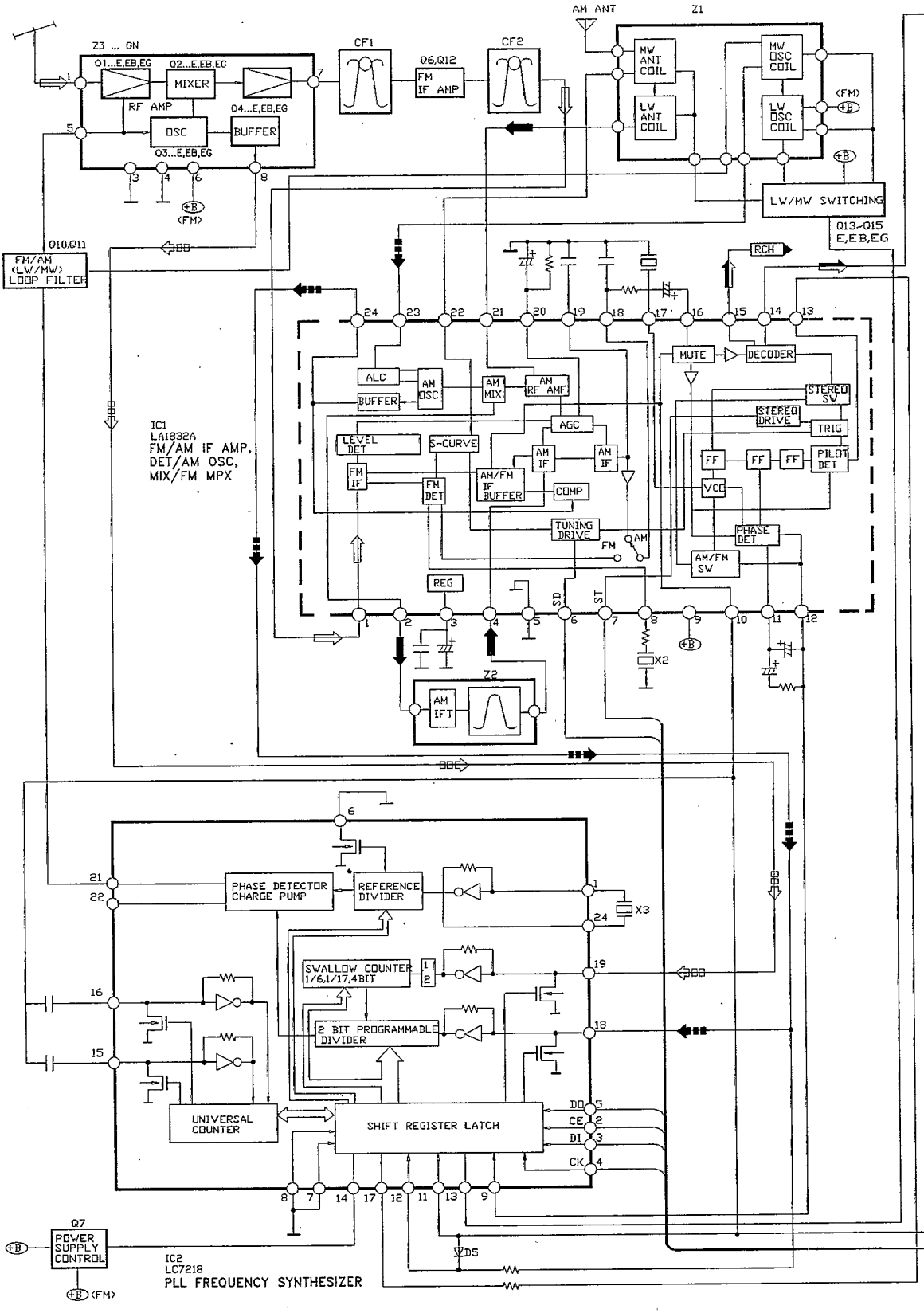
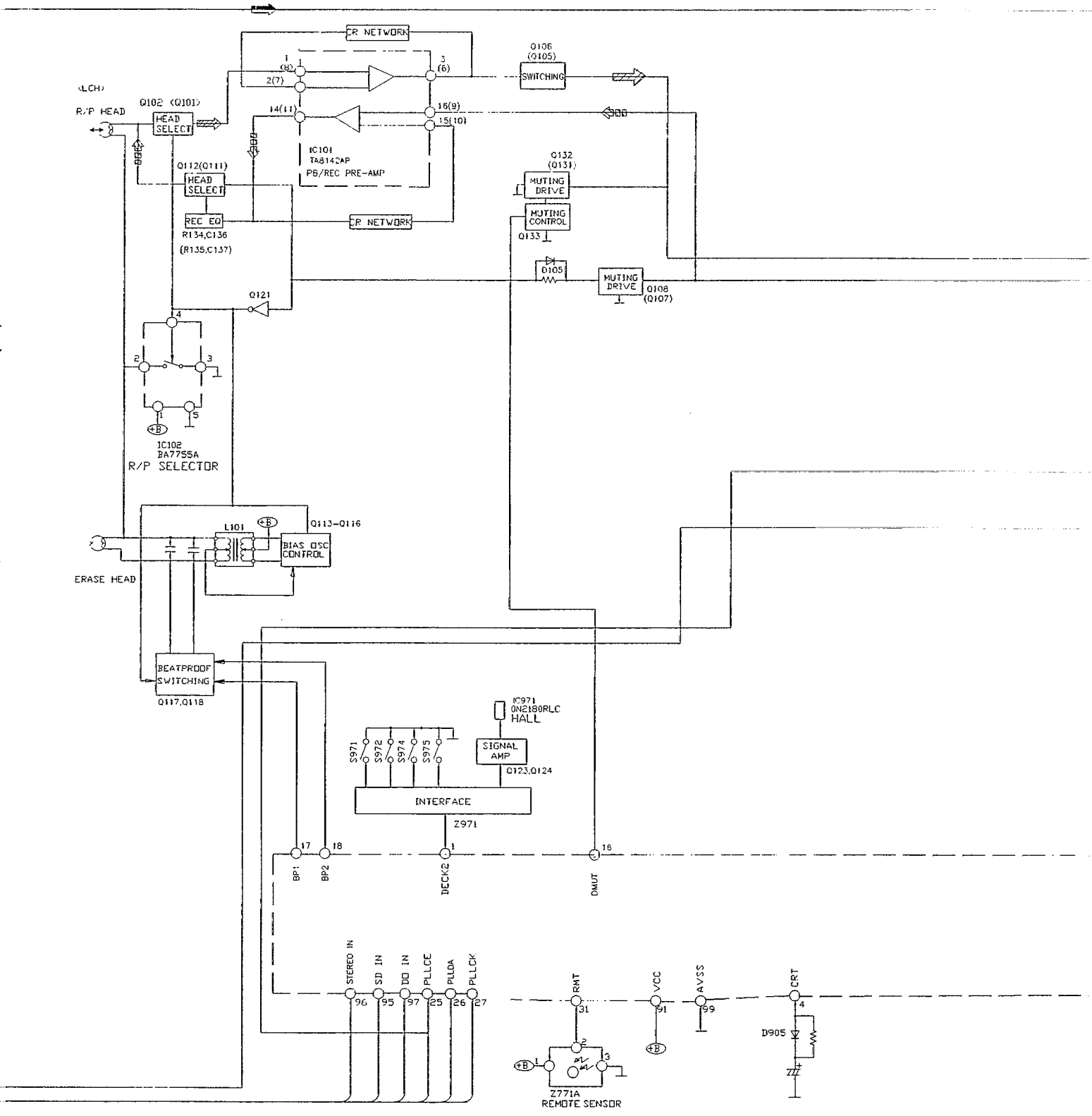
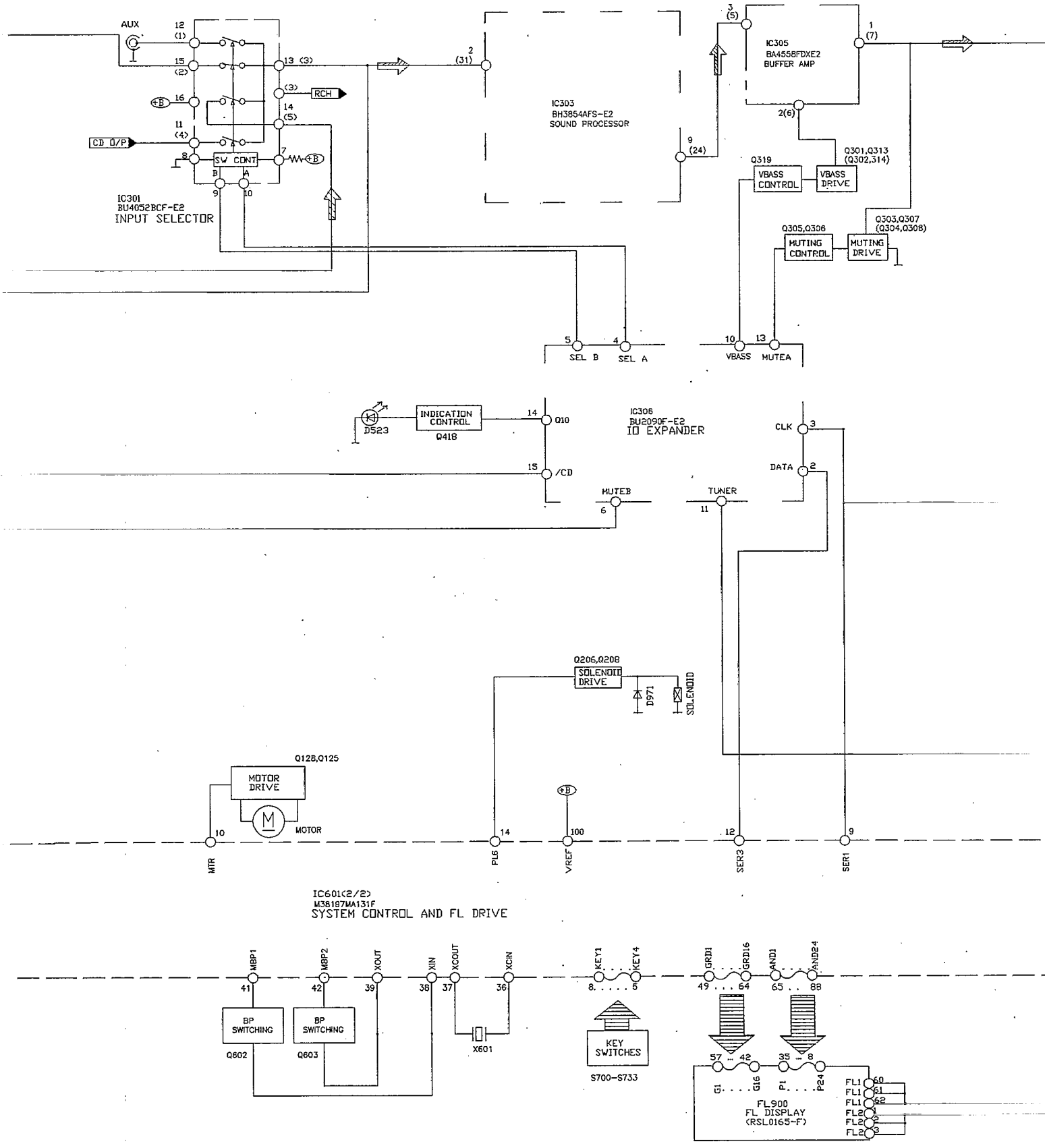
■ Block Diagram

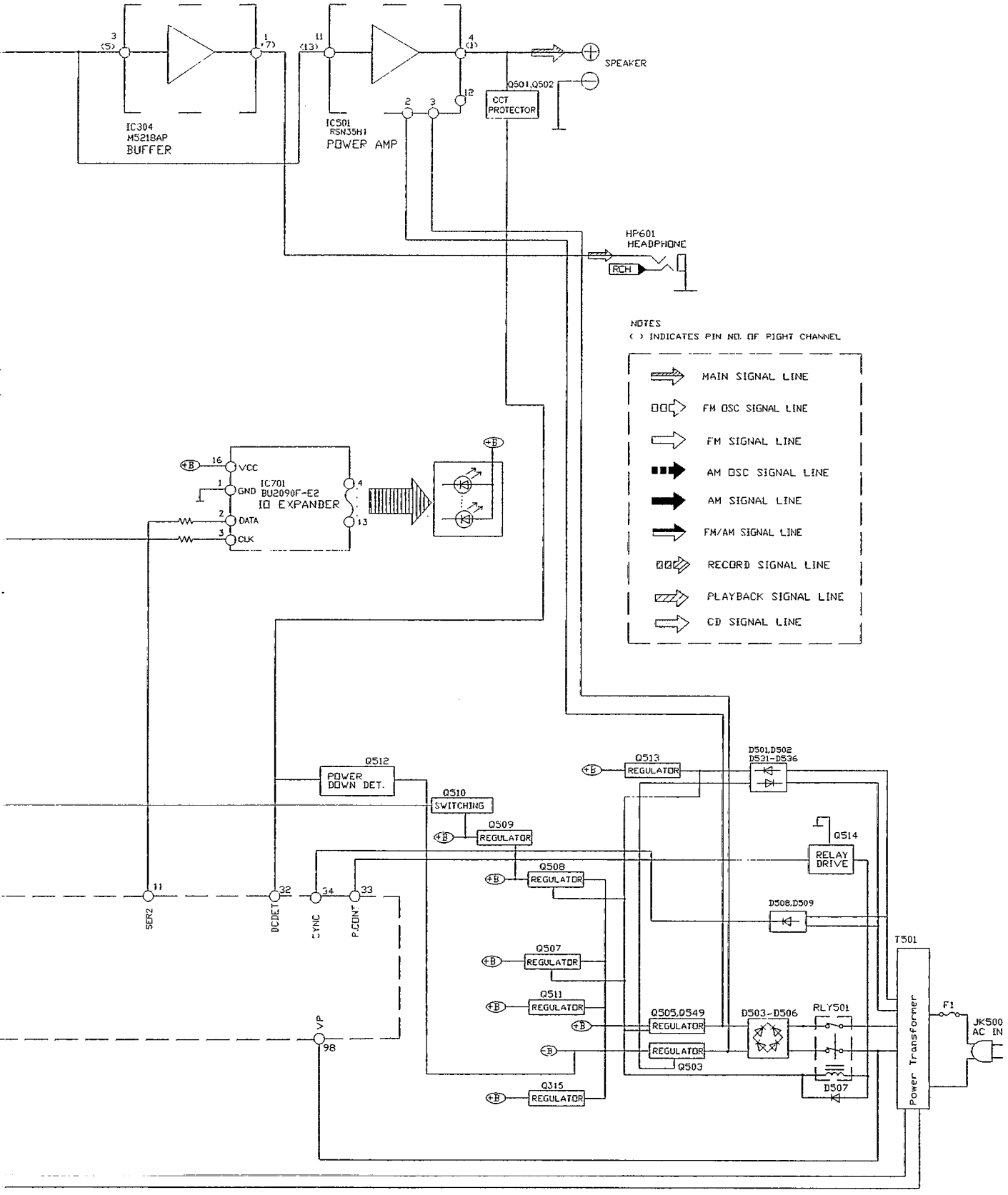



IC702
MN662741RPA
SERVO PROCESSOR/
DIGITAL FILTER/ DIGITAL SIGNAL
PROCESSOR/ D/A CONVERTER
IC401
UPD78043A042
SYSTEM CONTROL
IC601
M38197MA131F
SYSTEM CONTROL & FL CONTROL
CD O/P(Lch)
CD O/P(Rch)
Servo Input Port
A/D Converter
D/A Converter
Servo Output Port
Microcomputer Interface
Digital Audio Interface
Phase Detector
Frequency Comparator
VCO
DSL
Synchronizing Projector
EFM Data Demodulator
Synchronizing Interpolation Protection
16K SRAM
Peak Detector/ Auto cue
RAM address Generator
CLV Servo
Sub-code Demodulator
CRCC Check
Q Code Register
Servo CPU
Timing Generator
Syndrome Calculation
CIPC Decoder
Interpolation /Soft muting /Digital Attenuation
S/P Converter
Digital De-emphasis
Digital Filter
MATH Logic
PWM Logic
D511 Speed Sensor
D522 Position Sensor
D531 Single Sensor
D521 Disc Sensor
M511 (SLIDE MOTOR)
S501
S502
S503
X401
X701


AM ANT
Z1
Z3 ... GN
Q1...E,EB,EG
Q2...E,EB,EG
MIXER
RF AMP
OSC
BUFFER
Q4...E,EB,EG
Q3...E,EB,EG
CF1
CF2
Q6,Q12
FM IF AMP
MW ANT COIL
LW ANT COIL
MW OSC COIL
LW OSC COIL
(FM)
+B
LW/MW SWITCHING
Q13-Q15 E,EB,EG
Q10,Q11
FM/AM (LW/MW) LOOP FILTER
RCH
MUTE
DECODER
STEREO SW
STEREO DRIVE
TRIG
PILOT DET
FF
VCO
PHASE DET
AM/FM SW
ALC
AM OSC
BUFFER
AM MIX
AM RF AMP
AGC
LEVEL DET
S-CURVE
AM IF
FM IF
FM DET
AM/FM IF BUFFER
COMP
TUNING DRIVE
FM
AM
REG
SD
ST
X2
Z2
AM IFT
IC1
LA1832A
FM/AM IF AMP, DET/AM OSC, MIX/FM MPX
PHASE DETECTOR CHARGE PUMP
REFERENCE DIVIDER
X3
SWALLOW COUNTER 1/6,1/17,4BIT
2 BIT PROGRAMMABLE DIVIDER
UNIVERSAL COUNTER
SHIFT REGISTER LATCH
DO
CE
DI
CK
Q7
POWER SUPPLY CONTROL
D5
IC2
LC7218
PLL FREQUENCY SYNTHESIZER

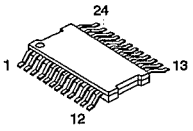

(LCH)
R/P HEAD
Q102 (Q101)
HEAD SELECT
Q112(Q111)
HEAD SELECT
REC EQ
R134,C136
(R135,C137)
CR NETWORK
IC101
TA8142AP
PB/REC PRE-AMP
CR NETWORK
Q106
(Q105)
SWITCHING
Q132
(Q131)
MUTING DRIVE
MUTING CONTROL
Q133
D105
MUTING DRIVE
Q108
(Q107)
Q121
IC102
BA7755A
R/P SELECTOR
L101
Q113-Q116
BIAS OSC CONTROL
ERASE HEAD
BEATPROOF SWITCHING
Q117,Q118
IC971
0N2180RLC
HALL
S971
S972
S974
S975
SIGNAL AMP
Q123,Q124
INTERFACE
Z971
BP1
BP2
DECK2
DMUT
STEREO IN
SD IN
DD IN
PLLCE
PLDA
PLLCK
RMT
VCC
AVSS
CRT
D905
Z771A
REMOTE SENSOR

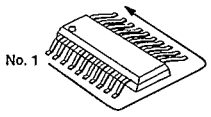

AUX
CD O/P
+B
SW CONT
RCH
IC301
BU4052BCF-E2
INPUT SELECTOR
IC303
BH3854AFS-E2
SOUND PROCESSOR
IC305
BA4558FDXE2
BUFFER AMP
Q319
VBASS CONTROL
VBASS DRIVE
Q301,Q313
(Q302,314)
Q305,Q306
MUTING CONTROL
MUTING DRIVE
Q303,Q307
(Q304,Q308)
SEL B
SEL A
VBASS
MUTEA
D523
INDICATION CONTROL
Q418
Q10
/CD
IC306
BU2090F-E2
IO EXPANDER
CLK
DATA
MUTEB
TUNER
Q206,Q208
SOLENOID DRIVE
D971
SOLENOID
Q128,Q125
MOTOR DRIVE
MOTOR
MTR
PL6
VREF
SER3
SER1
IC601(2/2)
M38197MA131F
SYSTEM CONTROL AND FL DRIVE
MBP1
MBP2
XOUT
XIN
XCOUT
XCIN
BP SWITCHING
Q602
Q603
X601
KEY1
KEY4
KEY SWITCHES
S700-S733
GRID1
GRID16
AND1
AND24
FL900
FL DISPLAY
(RSL0165-F)


IC304
M5218AP
BUFFER
IC501
RSNJ5H1
POWER AMP
SPEAKER
Q501,Q502
CCT PROTECTOR
HP601
HEADPHONE
RCH
NOTES
( ) INDICATES PIN NO. OF RIGHT CHANNEL
MAIN SIGNAL LINE
FM OSC SIGNAL LINE
FM SIGNAL LINE
AM OSC SIGNAL LINE
AM SIGNAL LINE
FM/AM SIGNAL LINE
RECORD SIGNAL LINE
PLAYBACK SIGNAL LINE
CD SIGNAL LINE
IC701
BU2090F-E2
IO EXPANDER
VCC
GND
DATA
CLK
Q512
POWER DOWN DET.
Q513
REGULATOR
D501,D502
D531-D536
Q510
SWITCHING
Q509
REGULATOR
Q514
RELAY DRIVE
Q508
REGULATOR
D508,D509
Q507
REGULATOR
Q511
REGULATOR
Q505,Q549
REGULATOR
REGULATOR
Q503
D503-D506
RLY501
D507
Q315
REGULATOR
T501
Power Transformer
F1
JK500
AC IN
SER2
DCDET
SYNC
P.CONT
VP

■ Terminal Guide of ICs, Transistors and Diodes

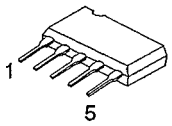
AN8389SE1

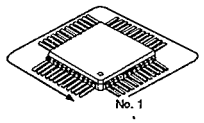




AN8835SBE1 (28P)
BU2090F-E2 (16P)
BU4052BCF-E2 (16P)
LA1832A (24P)
LC7218 (24P)
BH3854AFS-E2 (32P)

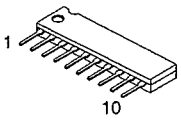
BA7755A



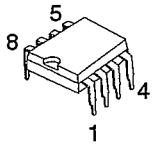


M38197MA131F(100P)
MN662741RPA (80P)
UPD78043A042 (80P)

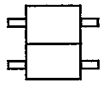
BA6247N



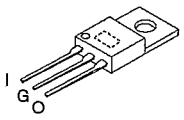
M5218AP



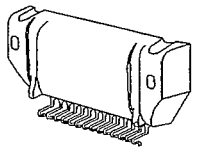
0N2180RLC



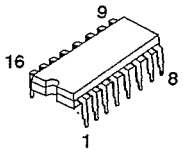
AN78M05



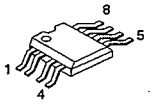
RSN35H1

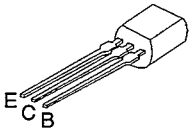


TA8142AP



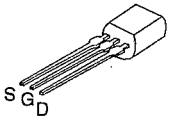
BA4558FDXE2



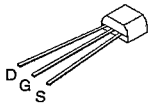


2SB621RTA
2SC2001KTA
2SD1302STA

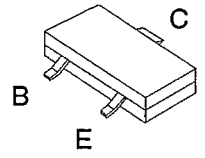
2SK301QTA

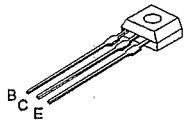


2SJ40CDTA



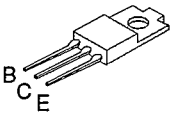
2SB709S



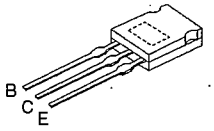


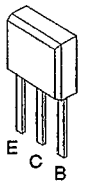
2SC2785FETA
2SD1020HTA
2SC2785FTA
2SC2787LTA
BN1L3NTA
BA1F4MTA

2SB1185E
2SD1762E

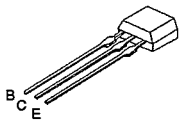


2SD2037ETA





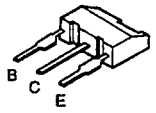
2SC2784FTA
BA1L4ZTA
2SD1450STA
2SC3311AIQST

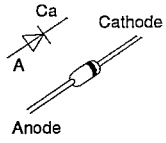


RVTDTA143XST
2SA933SSTA
2SC1740SSTA
RVTDTA114EST

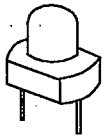
RVTDTC114TST
RVTDTC124EST
RVTDTA124EST
RVTDTC114EST

2SB1320AQRTA

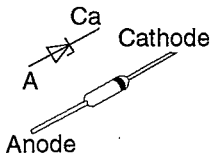




RVD1SS133TA
1SS291TA
MA165TA
MA167TA



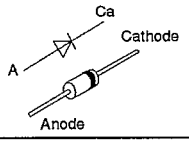
LNJ301MPUJAD
SLR-325MC
SLR-325VC



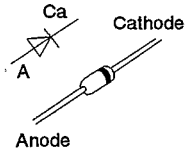
MTZJ12BTA
MTZJ15CTA
MTZJ5R6CTA
MTZJ6R2CTA
MTZJ6R8BTA
MTZJ5R1BTA
MTZJ5R6BTA

MTZJ10BTA
MTZJ3R6BTA
MTZJ5R1CTA
MTZJ7R5CTA
MTZJ8R2CTA
MTZJ9R1CTA

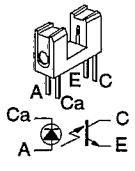
1N5402BM21
1D3E
RL154M11



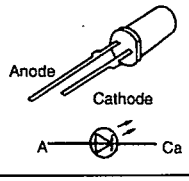
MA165



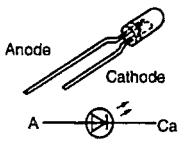
RSQGP1S53V

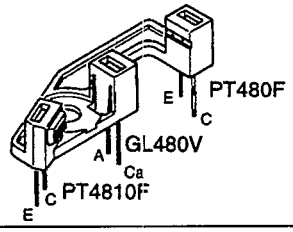


LN66S



BR3433S





■ Terminal Function of ICs

• IC701 (AN8835SBE1) Servo Amplifier

Pin No.	Mark	I/O	Function
1	PDA	I	Focus signal input terminal 1 (Ach).
2	PDB	I	Focus signal input terminal 2 (Bch).
3	VCC	I	Power supply terminal.
4	LPD	I	Laser PD signal.
5	LD	O	Laser power auto control output.
6	RF	O	RF amplifier terminal.
7	RF IN	I	AGC input terminal.
8	CAGC	I	AGC detection capacitor input.
9	ARF	O	RF output
10	CSBRT	I	OFTR capacitor connection terminal.
11	CEA	I	HPF-AMP capacitor connection terminal.
12	BDO	O	Dropout detection control.
13	LDON	I	LD APC ON/OFF("H" : ON, "L" : OFF)
14	GND	—	GND terminal.

Pin No.	Mark	I/O	Function
15	/RFDET	O	RF detection signal ("L" : detection).
16	CROSS	O	Tracking error zero cross output.
17	OFTR	O	Off track detection ("H" : detection).
18	VDET	O	Oscillation detection signal ("H" : detection).
19	ENV	O	Envelope output terminal
20	TEBPF	I	Oscillation det. input terminal (Not used,open)
21	CCRS	I	CROSS capacitor connection terminal.
22	TE	O	Tracking error signal.
23	FE	O	Focus error signal.
24	TBAL	I	Tracking balance adjusting input
25	FBAL	I	Focus balance adjusting input
26	VREF	O	Reference voltage output
27	PDE	I	Tracking signal input terminal 1 (Ech).
28	PDF	I	Tracking signal input terminal 2 (Fch).

• IC703 (AN8389SE1) Focus coil / Tracking coil / Traverse motor / Spindle motor driver

Pin No.	Mark	I/O	Function
1	VCC	I	Power supply terminal
2	VREF	I	Reference voltage input
3	IN4	I	Motor driver (4) input
4	IN3	I	Motor driver (3) input
5	GND	—	Ground connection
6	NC	—	Ground connection
7	NRESET	I	Reset input
8	GND	—	Ground connection
9	IN2	I	Motor driver (2) input
10	PC2	I	PC2 (power cut) input
11	IN1	I	Motor driver (1) input
12	PC1	I	PC1 (power cut) input (Not used, open)

Pin No.	Mark	I/O	Function
13	PVCC1	I	Power supply (1) for driver
14	PGND1	—	Ground connection (1) for driver
15	D1–	O	Motor driver (1) reverse-action output
16	D1+	O	Motor driver (1) forward-action output
17	D2–	O	Motor driver (2) reverse-action output
18	D2+	O	Motor driver (2) forward-action output
19	D3–	O	Motor driver (3) reverse-action output
20	D3+	O	Motor driver (3) forward-action output
21	D4–	O	Motor driver (4) reverse-action output
22	D4+	O	Motor driver (4) forward-action output
23	PGND2	—	Ground connection (2) for driver
24	PVCC2	I	Power supply (2) for driver

• IC702 (MN662741RPA) Servo processor / Digital signal processor / Digital filter / D/A converter

Pin No.	Mark	I/O	Function
1	BCLK	O	Serial bit clock terminal (Not used, open)
2	LRCK	O	L/R discriminating signal (Not used, open)
3	SRDATA	O	Serial data (Not used, open)
4	DVDD1	I	Power supply (digital circuit) terminal
5	DVSS1	—	GND (digital circuit) terminal
6	TX	O	Digital audio interface signal
7	MCLK	I	Microprocessor command clock signal
8	MDATA	I	Microprocessor command data signal
9	MLD	I	Microprocessor command load signal
10	SENSE	O	Sense signal output
			(OFT,FESL,MAGEND,NAJEND,POSAD,SFG)
11	/FLOCK	O	Optical servo condition(focus)("L" : lead-in)
12	/TLOCK	O	Optical servo condition(tracking)("L" : lead-in)
13	BLKCK	O	Sub-code block clock (f=75Hz)
14	SQCK	I	External clock signal input for sub-code Q
			register.
15	SUBQ	O	Sub-code Q code output
16	DMUTE	I	Muting input ("H" : mute)
17	STAT	O	Status signal output
			(CRC,CUE,CLVS,TTSTVP,FCLV,SQCK)
18	/RST	I	Reset input
19	SMCK	O	1/2-divided clock signal of crystal oscillating at
			MSEL = "H" (fSMCK=8.4672MHz)
			1/4-divided clock signal of crystal oscillating at
			MSEL="L" (fSMCK=4.2336MHz)
20	PMCK	O	1/192-divided clock signal of crystal oscillating
			(fPMCK=88.2kHz) (Not used, open)
21	TRV	O	Traverse servo control output
22	TVD	O	Traverse drive signal output
23	PC	O	Spindle motor ON signal output ("L" : ON)
24	ECM	O	Spindle motor drive signal output
			(forced mode output)
25	ECS	O	Spindle motor drive signal output
			(servo error signal output)
26	KICK	O	Kick pulse output
27	TRD	O	Tracking drive output
28	FOD	O	Focus drive output
29	VREF	I	D/A (drive) output (TVD,ECS,TRD,FOD,
			FBAL,TBAL) Reference voltage input.
30	FBAL	O	Focus balance adjustment output
			(Not used,open)
31	TBAL	O	Tracking balance adjustment output
32	FE	I	Focus error signal input (analog input)
33	TE	I	Tracking error signal input (analog input)
34	RFENV	I	RF envelope signal input
35	VDET	I	Vibration detection signal input ("H" : detection)

Pin No.	Mark	I/O	Function
36	OFT	I	Off-track signal input ("H" : off track)
37	TRCRS	I	Track cross signal input
38	/RFDET	I	RF detection signal input ("L" : detection)
39	BDO	I	Dropout signal input ("H" : Dropout)
40	LDON	O	Laser on signal output ("H" : ON)
41	TES	O	Tracking error shunt signal output ("H" : shunt)
42	PLAY	O	Play signal out ("H" : PLAY)
43	WVEL	O	Double speed status signal output ("H" : DS)
44	ARF	I	RF signal input
45	IREF	I	Reference current input
46	DRF	I	DSL bias (Not used, open)
47	DSLF	I/O	DSL loop filter
48	PLLF	I/O	PLL loop filter
49	VCOF	I/O	VCO loop filter (Not used, open)
50	AVDD2	I	Power supply input (for analog circuit)
51	AVSS2	—	GND (for analog circuit)
52	EFM	O	EFM signal output (Not used, open)
53	PCK	O	PLL extraction clock ouput (Not used, open)
			(fPCK=4.321 MHz during normal playback)
54	PDO	O	Phase comparison signal of EFM and PCK signals
			(Not used, open)
55	SUBC	O	Sub-code serial data output (Not used, open)
56	SBCK	I	Sub-code frame clock signal output
			(fCLDCK=7.35kHz during normal playback)
57	VSS	—	GND
58	X1	I	Crystal oscillating circuit input (f=16.9344MHz)
59	X2	O	Crystal oscillating circuit output (f=16.9344MHz)
60	VDD	I	Power supply input (for oscillating circuit)
61	BYTCK	O	Byte clock output (Not used, open)
62	/CLDCK	O	Clock input for sub-code serial data
			(Not used, open)
63	FCLK	O	Crystal frame clock signal output
			(fCLK=7.35kHz, double=14.7kHz)
64	IPFLAG	O	Interpolation flag output ("H" : interpolation)
			(Not used, open)
65	FLAG	O	Flag output (Not used, open)
66	CLVS	O	Spindle servo phase synchronizing signal output
			("H" : CLV, "L" : rough servo) (Not used, open)
67	CRC	O	Sub-code CRC checked output
			("H" : OK, "L" : NG) (Not used, open)
68	DEMPH	O	De-emphasis ON signal output
			("H" : ON) (Not used, open)
69	RESY	O	Frame resynchronizing signal output
			(Not used, open)
70	/RST2	I	Reset input through MASH circuit ("L" : Reset)
71	/TEST	I	Test input

Pin No.	Mark	I/O	Function
72	AVDD1	I	Power supply input (for analog circuit)
73	OUTL	O	Left channel audio signal output
74	AVSS1	—	GND
75	OUTR	O	Right channel audio signal output
76	RSEL	I	RF signal polarity assignment input
			(at "H" level, RSEL="H", at "L" level, RESL="L")
77	CSEL	I	Crystal oscillating frequency designation input

Pin No.	Mark	I/O	Function
			"L" : 16.9344MHz "H" : 33.8688MHz
78	PSEL	I	Test input (normally "L") (Not used, open)
79	MSEL	I	Output mode switching of SUBQ terminal
			("H" : Q code buffer mode)
80	SSEL	I	Output frequency switching for SMCK terminal
			"H" : SMCK=8.4672MHz
			"L" : MCK=4.2336MHz (Not used, open)

• IC401 (UPD78043A042) System Control

Pin No.	Mark	I/O	Function
1~6	NC	—	Not connected.
7	LIGHT	—	Not connected.
8	VDD	I	Power input.
9	SCK	O	Serial clock output.
10	SDO	—	Not connected.
11	SDI	I	Serial data input.
12	/CS	O	Chip select.
13	DMUTE	O	Muting control.
14	SQCK	O	Sub code Q resistor clock output.
15	NC	—	Not connected.
16	SUBQ	I	Sub code Q data input.
17	/RESET	I	Reset signal input.
18	KBCLK	—	Not connected.
19	KBDATA	—	Not connected.
20	AVSS	—	GND.
21	/RSTSV	O	Reset signal output.
22	CDREQ	O	CD request signal output.
23	DIR	O	Motor control signal.
24	SLIDE	O	Motor control signal output.
25	LOAD	O	Motor control signal.
26	NC	—	Not connected.
27	H-60	—	No use (connect to power).
28	NC	—	Not connected.
29	AVDD	I	Power input.
30	AVREF	I	GND.
31	XT1	—	GND.
32	XT2	—	Not connected.
33	VSS	—	GND.
34	X1	I	Ceramic oscillator (f=4.2336MHz).
35	X2	O	Ceramic oscillator (f=4.2336MHz).
36	MCLK	O	Command clock signal output.

Pin No.	Mark	I/O	Function
37	MDATA	O	Command data signal output.
38	MLD	O	Command load signal output ("L" : Load).
39~42	NC	—	Not connected.
43	PWM	O	Motor control signal output.
44	POFF	O	GND.
45	POSITION	I	Tray position detection input.
46	SPEED	I	Loading motor speed sensor.
47	REMOCON	I	GND.
48	IC	—	GND.
49	/EPHOLD	—	Not connected.
50	EPSO	—	Not connected.
51	EPCLK	—	Not connected.
52	VDD	I	Power input.
53	POWER	—	Not connected.
54	EPSI	—	Not connected.
55	/EPCS	—	Not connected.
56	SINGLE	I	Disc slot detection (Single play).
57	DISC	I	Disc control signal input.
58	MLOCK	I	Mechanism detection (S501).
59	CLAMP	I	Mechanism detection (S502).
60	FREE	I	Mechanism detection (S503).
61	NC	—	Not connected.
62	STAT	I	Status signal input.
63	REST	I	Rest position detection.
64	MSC	—	Not connected.
65	STP1	—	Connect to GND through resistor.
66	STP2	—	Connect to GND through resistor.
67~70	NC	—	Not connected.
71	VPP	—	GND.
72~80	NC	—	Not connected.

• IC601 (M38197MA131F) System Microprocessor

Pin No.	Mark	I/O	Function
1	DECK	I	Mecha condition input. (HALF / RECINH_F / RECINH_R / MODE)
2	PHOTO	I	Counter detector.
3	NC	—	GND
4	CRT	I	CRT input.
5~8	KEY4 ~ KEY1	I	Key switch input.
9	SER1	O	Serial clock (EX1 CLK, EX2 CLK)
10	MTR	O	Motor control. (Volume)
11	SER2	O	Serial data/clock(EX1 DAT, GEC DAT)
12	SER3	O	Serial data (EX2 DAT, GEC CLK).
13	SER4	O	Serial data (GEC LATCH).
14	PLG	O	Planger control.
15	REC_L	O	Record low swtiching control.
16	DMUT	O	Deck mute output.
17	BP1	O	Beatproof output 1.
18	BP2	O	Beatproof output 2.
19	CS	I	CD CS.
20	CLK1	I	CD clock input.
21	SO1	O	CD data output.
22	SI1	I	CD data input.
23	REQ	I/O	CD request.
24	MCRST	O	MCRST.
25	/PLLCE	O	/Tuner PLL chip enable.
26	/PLLDA	O	/Tuner PLL data output.
27	/PLLCK	O	/Tuner clock output.
28	MIC SW	O	MIC jack SW on/off
29	NC	—	GND
30	CD MPCN	O	MECHA control power.
31	RMT	I	Remote control signal input.

Pin No.	Mark	I/O	Function
32	DCDET	I	DC detect input.
33	P.CONT	O	Power control signal.
34	SYNC	I	AC failure detect input.
35	RESET	I	Reset input.
36	XCIN	I	32.768 sub clock
37	XCOUT	O	
38	XIN	I	6MHz main clock
39	XOUT	O	6MHz main clock.
40	VSS	—	GND
41	MBP1	O	MPU beat proof output 1.
42	MBP2	O	MPU beat proof output 2.
43	CDGMUTE	—	NC
44	/CDGRESET	—	NC
45~48	NC	—	NC
49~64	DIG1 ~ 16	O	Digit drive output (GRID).
65~80	SEG1 ~16	O	Segment drive output (ANODE).
81~88	SEG17 ~ 24	O	Segment drive output (ANODE) and key scan ouput.
89	JOG A	I	JOG input A.
90	JOG B	I	JOG input B.
91	VCC	—	Power (+5V).
92	REG IN	I	Area setting input.
93~94	NC	—	NC
95	SD IN	I	Tuner signal detection input.
96	STEREO IN	I	Tuner stereo detection input.
97	DO IN	I	Tuner PLL IF data input.
98	VP	—	Power (–30V).
99	AVSS	—	Power (0V)
100	VREF	—	Reference A-D.

■ Schematic Diagram

(All schematic diagrams may be modified at any time with the development of new technology)

Note :

- **S501** : Lock detect switch.
- **S502** : Clamp detect switch.
- **S503** : Clamp detect switch.
- **S700** : CD switch.
- **S701** : Reset switch.
- **S701** : Single play switch.
- **S702** : CD edit switch.
- **S703** : Group A switch.
- **S704** : Group B switch.
- **S705** : Group C switch.
- **S706** : Group D switch.
- **S707** : Group E switch.
- **S708** : Group F switch.
- **S709** : Group mode switch.
- **S710** : Group enter switch.
- **S711** : Group name enter switch.
- **S712** : Disk skip / Group name (+) switch.
- **S713** : Disk skip / Group name (–) switch.
- **S715** : V. Bass switch.
- **S716** : EQ. Space switch.
- **S717** : AUX switch.
- **S718** : Tuner select switch.
- **S719** : CD select switch.
- **S720** : Tape select switch.
- **S723** : REC. start switch.
- **S724** : REV. mode switch.
- **S725** : Timer REC. / Play switch.
- **S726** : Clock / Timer switch.
- **S727** : Power switch.
- **S728** : Memory / Set switch.
- **S729** : REV. / Down switch.
- **S730** : Stop / Tuning mode switch.
- **S731** : FF / Up switch.
- **S732** : FM Mode / BP select switch.
- **S733** : Deck open switch.
- **S971** : Deck mode detect switch.
- **S972** : Deck tape detect switch.
- **S973** : Deck CrO_2 detect switch.
- **S974** : Deck record detect switch.
- **S975** : Deck record detect switch.
- **VR501** : CD sensor adjustment.
- **VR603** : Jog volume control.

• **Signal line**

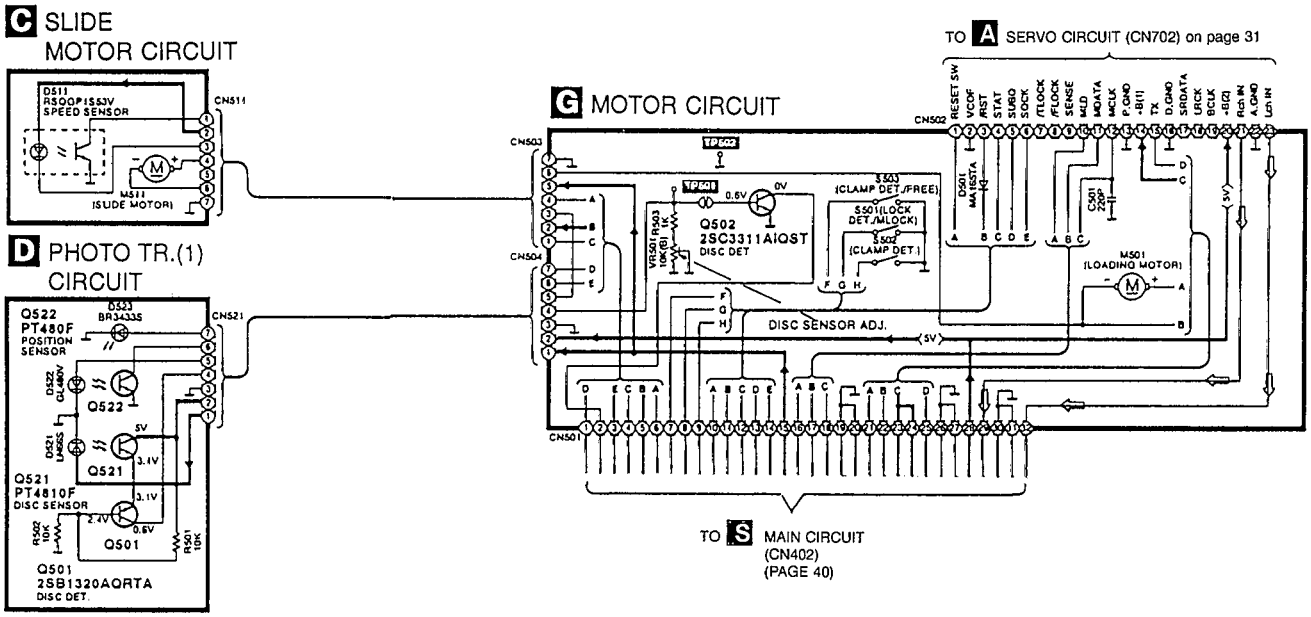
: +B line
: –B line
: FM/AM signal line
: Main signal line
: Playback signal line
: Record signal line
: CD signal line
: FM signal line
: AM signal line
: AM OSC signal line
: FM OSC signal line
: Aux signal line

•The voltage value and waveforms are the reference voltage of this unit measured by DC electronic voltmeter (high impedance) and oscilloscope on the basis of chassis.
Accordingly, there may arise some error in voltage values and waveforms depending upon the internal impedance of the tester or the measuring unit.

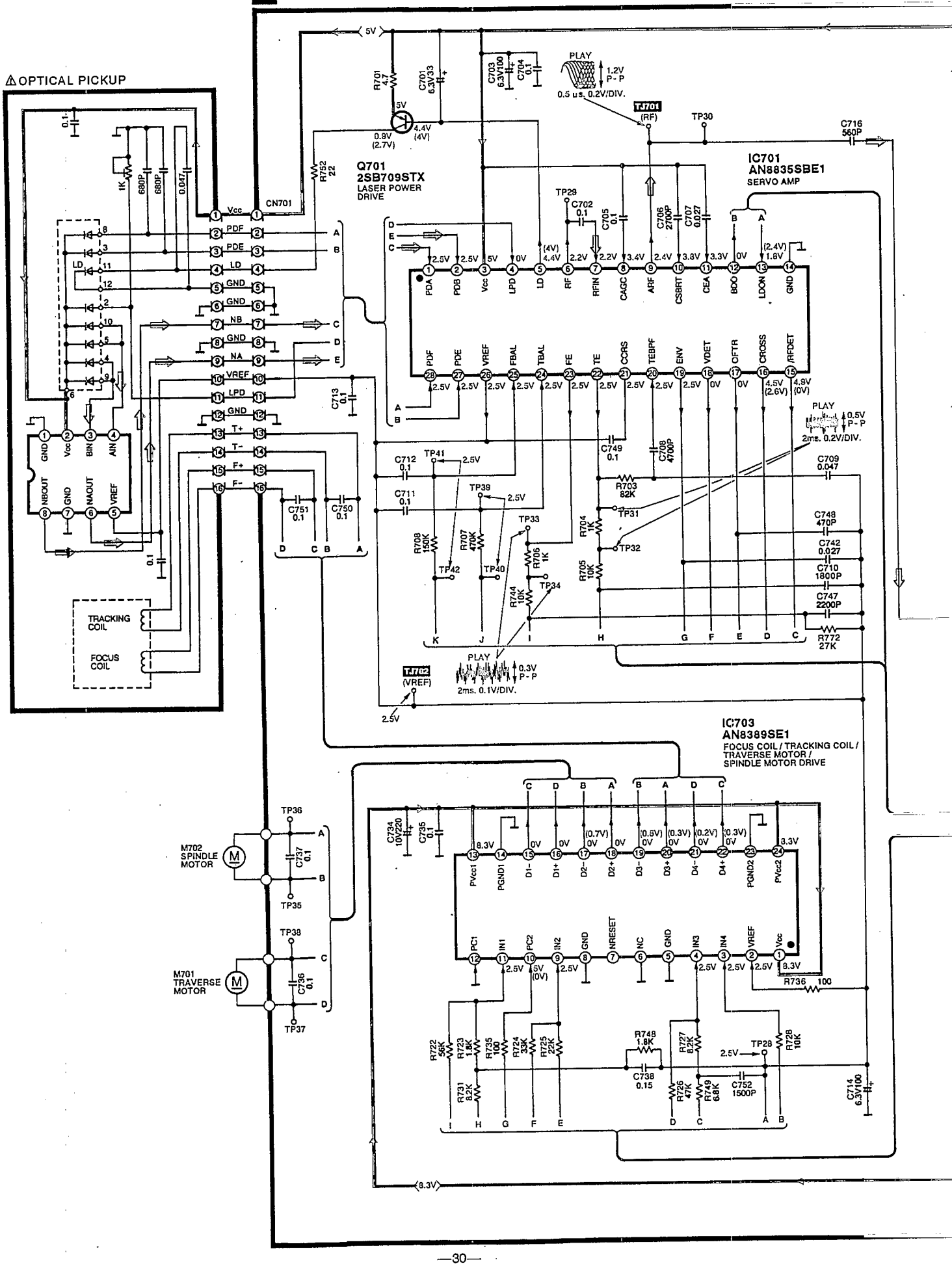
No mark : Playback << >>.....Tape Recording (( )) : CD ( ) ..... AM < > ..... FM

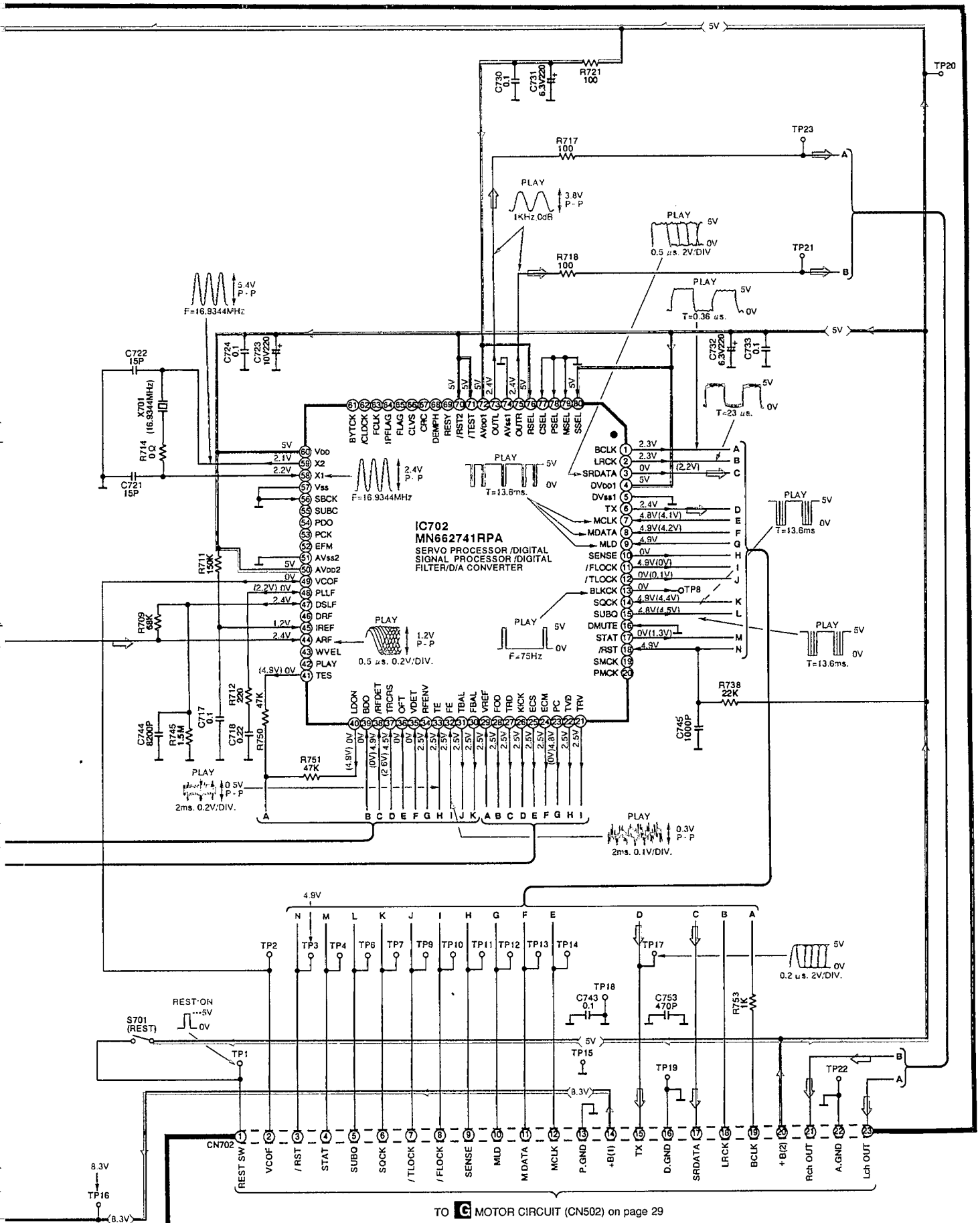
•Importance safety notice:
Components identified by ⚠ mark have special characteristics important for safety. Furthermore, special parts which have purposes of fire-retardant (resistors), high-quality sound (capacitors), low-noise (resistors), etc. are used. When replacing any of components, be sure to use only manufacturer's specified parts shown in the parts list.

Caution !
IC, LSI and VLSI are sensitive to static electricity.
Secondary trouble can be prevented by taking care during repair.
•Cover the parts boxes made of plastics with aluminium foil.
•Ground the soldering iron.
•Do not touch the pins of IC, LSI or VLSI with fingers directly.
•Put a conductive mat on the work table.

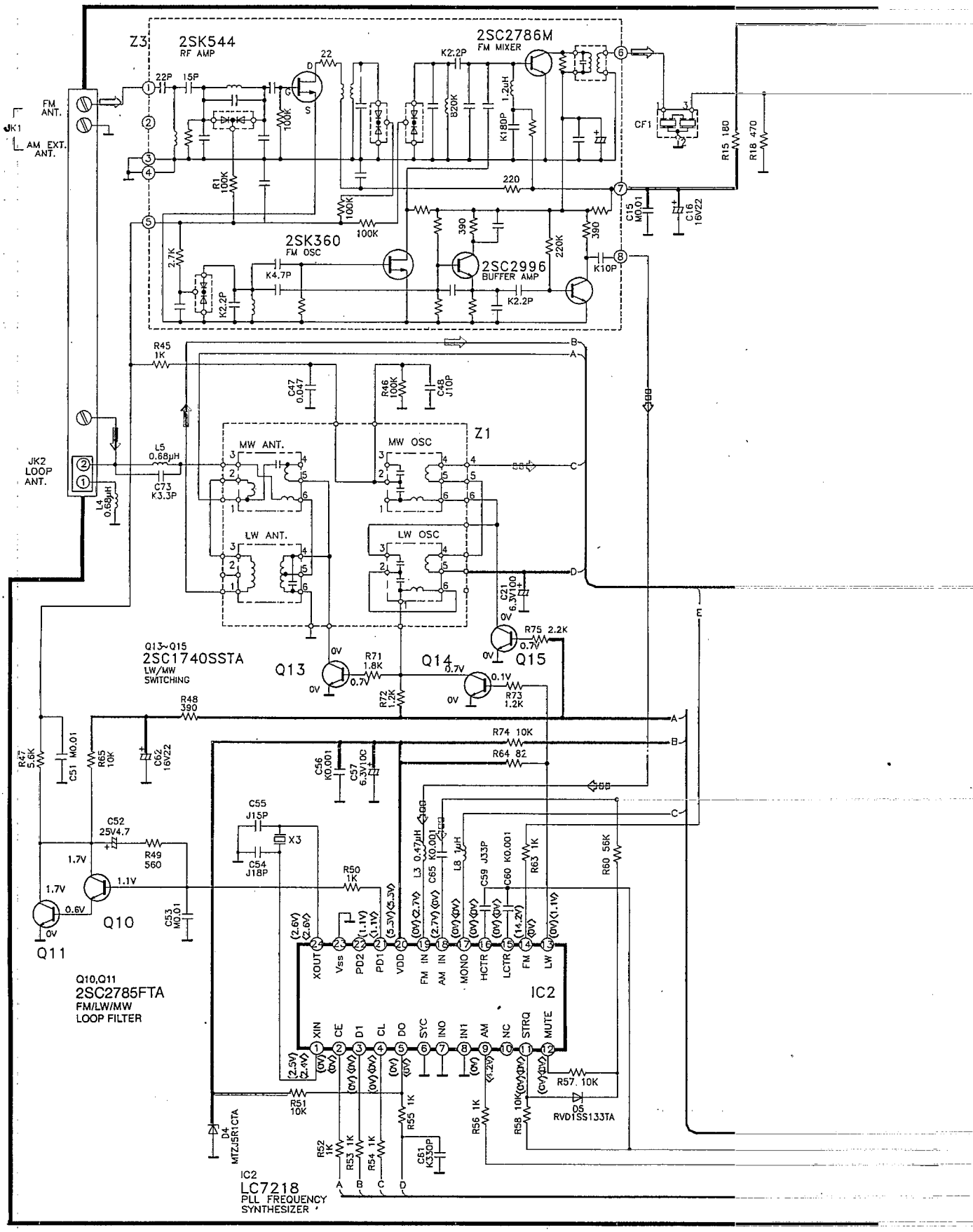


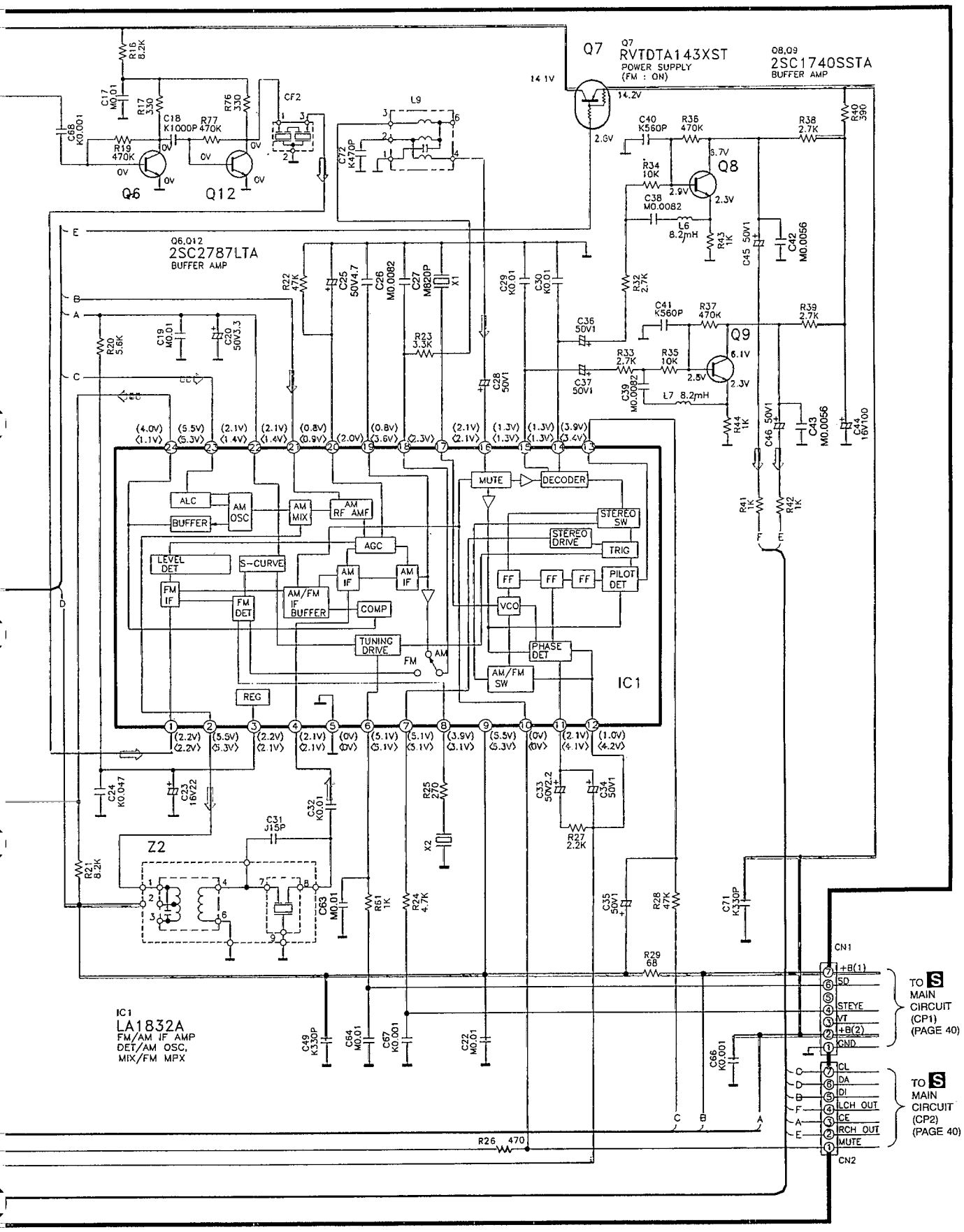
A SERVO CIRCUIT (P.C. Board: on page 43)



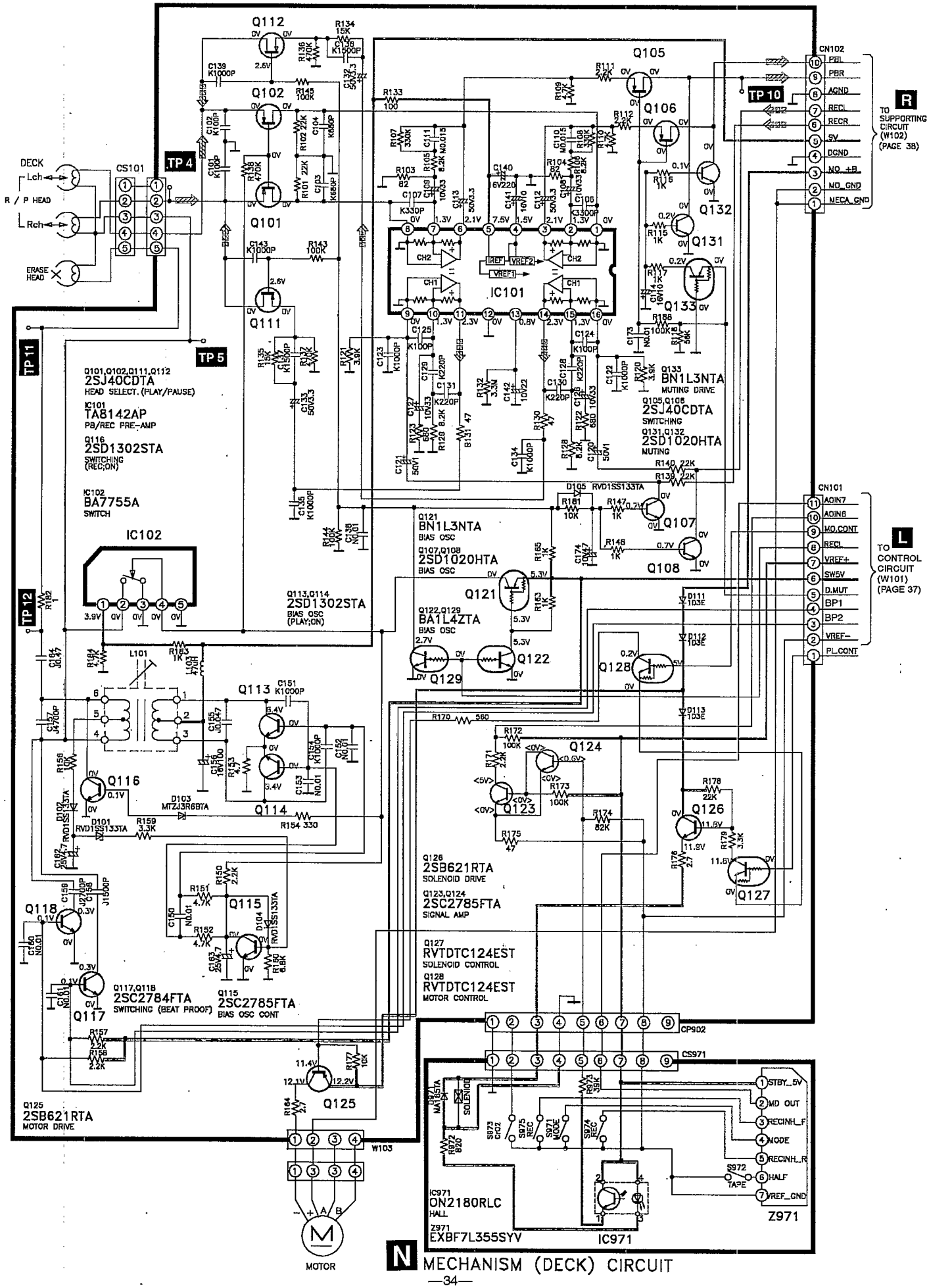

IC702
MN662741RPA
SERVO PROCESSOR /DIGITAL SIGNAL PROCESSOR /DIGITAL FILTER/D/A CONVERTER
CN702
REST SW
VCOF
/ RST
STAT
SUBQ
SQCK
/ TLOCK
/ FLOCK
SENSE
MLD
M.DATA
MCLK
P.GND
+B(I)
TX
D.GND
SRDATA
LRCK
BCLK
+ B(2)
Rch OUT
A.GND
Lch OUT
S701 (REST)
REST-ON
TO G MOTOR CIRCUIT (CN502) on page 29

B TUNER CIRCUIT

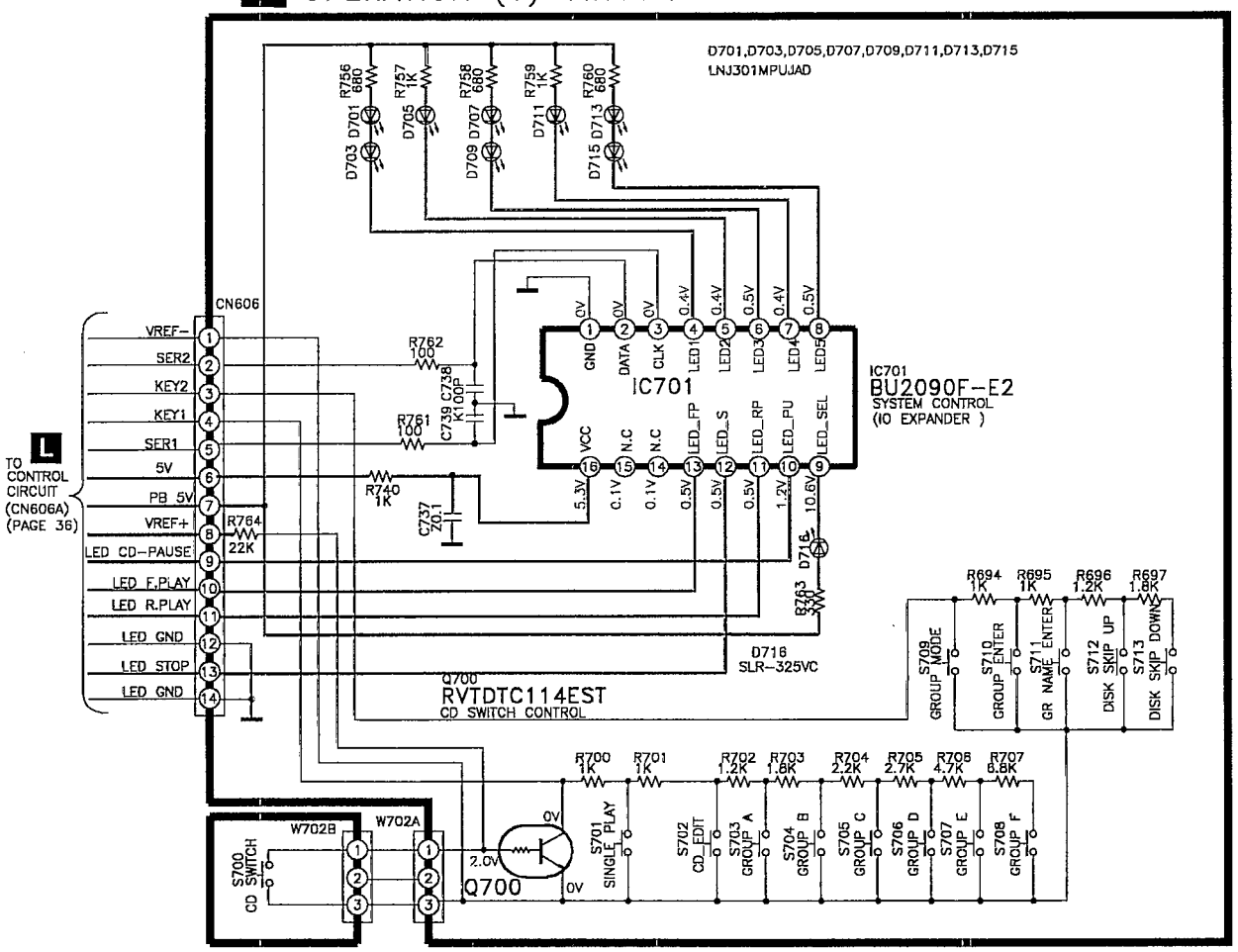



Q7
RVTDTA143XST
POWER SUPPLY
(FM : ON)
Q8,Q9
2SC1740SSTA
BUFFER AMP
Q6,Q12
2SC2787LTA
BUFFER AMP
IC1
LA1832A
FM/AM IF AMP
DET/AM OSC,
MIX/FM MPX
MUTE
DECODER
STEREO SW
STEREO DRIVE
TRIG
PILOT DET
VCO
PHASE DET
AM/FM SW
TUNING DRIVE
AM OSC
AM MIX
AM RF AMP
AGC
LEVEL DET
S-CURVE
AM IF
FM IF
FM DET
AM/FM IF BUFFER
COMP
ALC
BUFFER
REG
FF
CN1
+B(1)
SD
STEYE
VT
+B(2)
GND
CL
DA
DI
LCH OUT
CE
RCH OUT
MUTE
CN2
TO S MAIN CIRCUIT (CP1) (PAGE 40)
TO S MAIN CIRCUIT (CP2) (PAGE 40)

O DECK CIRCUIT

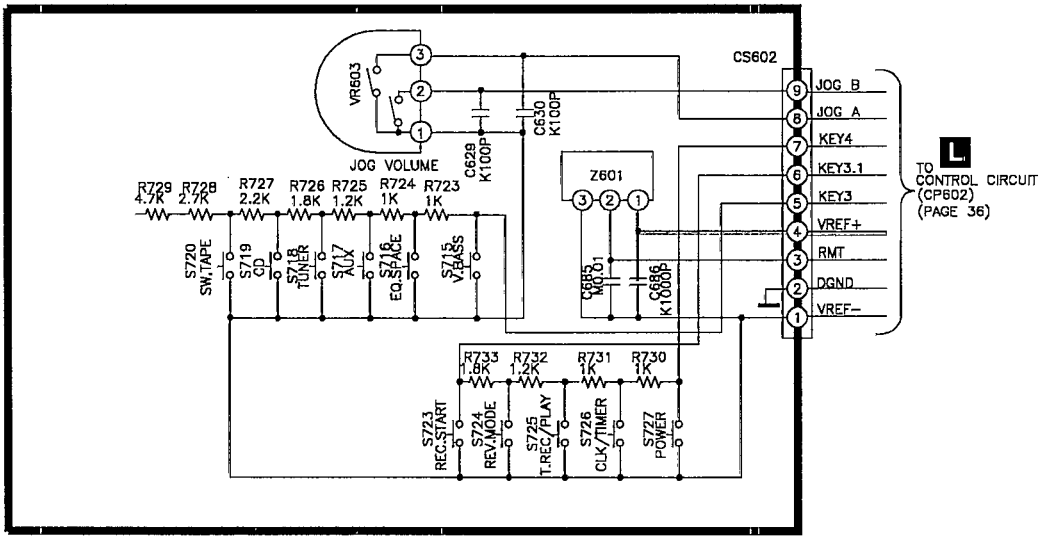


F OPERATION (1) CIRCUIT

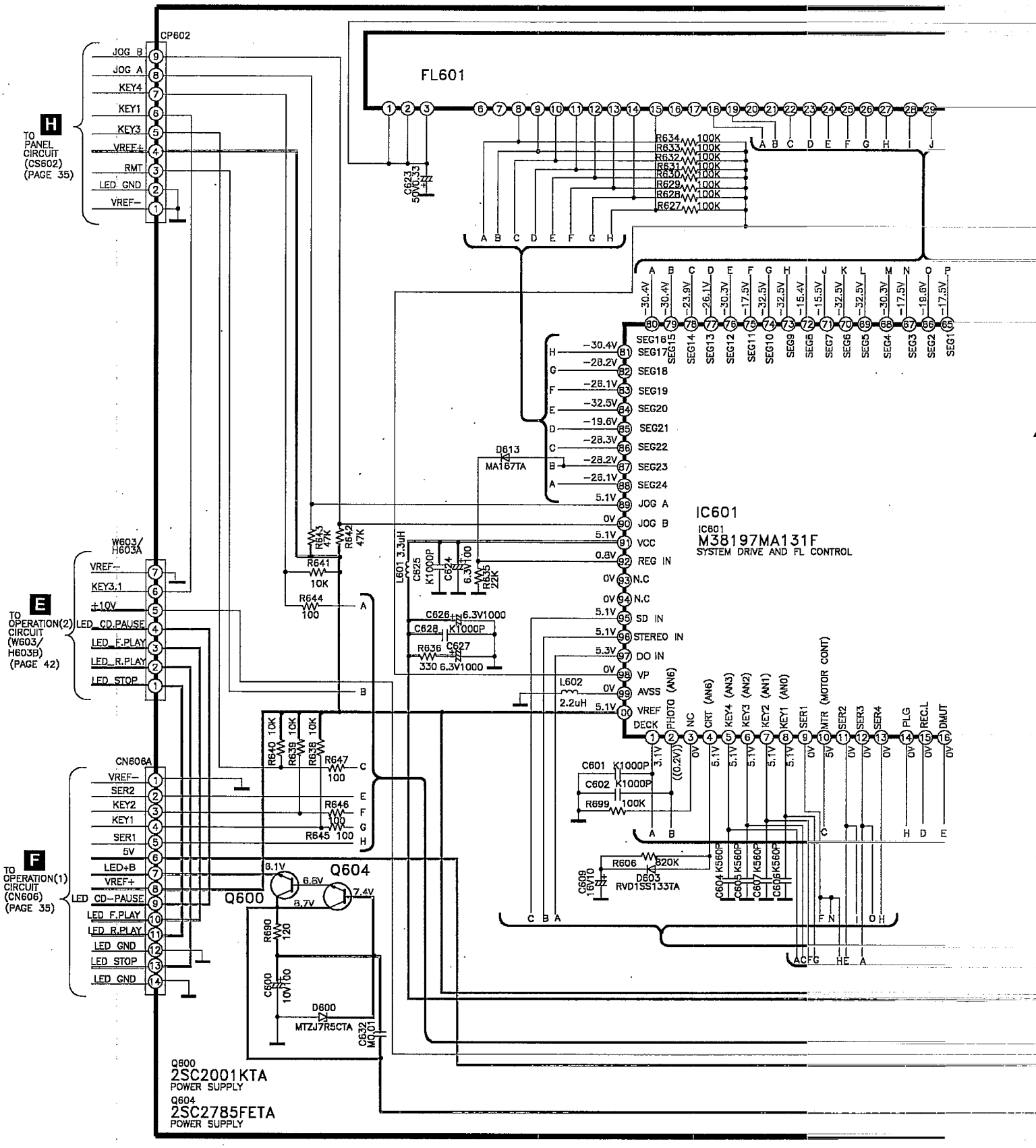


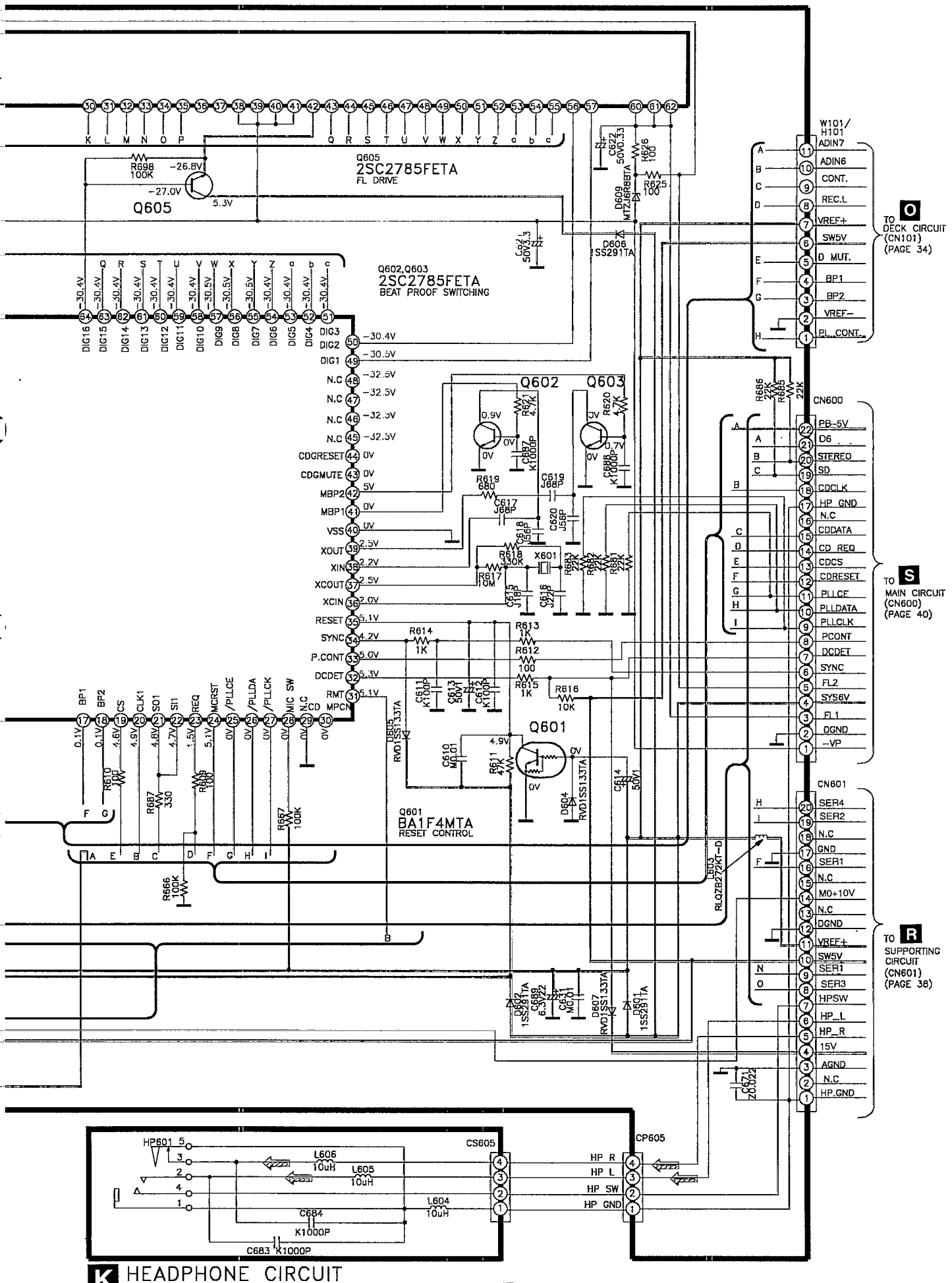
Q CD SWITCH CIRCUIT

H PANEL CIRCUIT



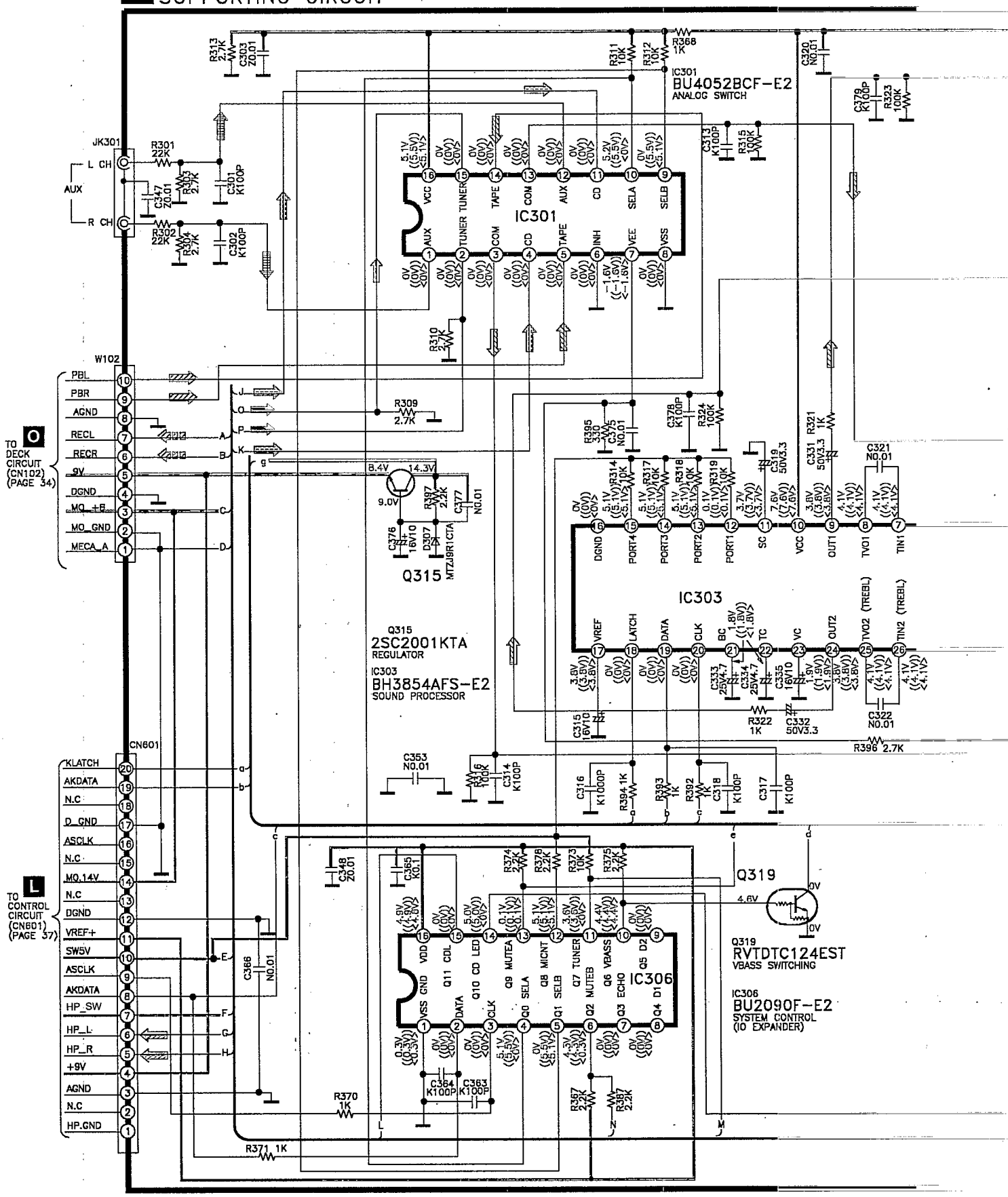
L CONTROL CIRCUIT

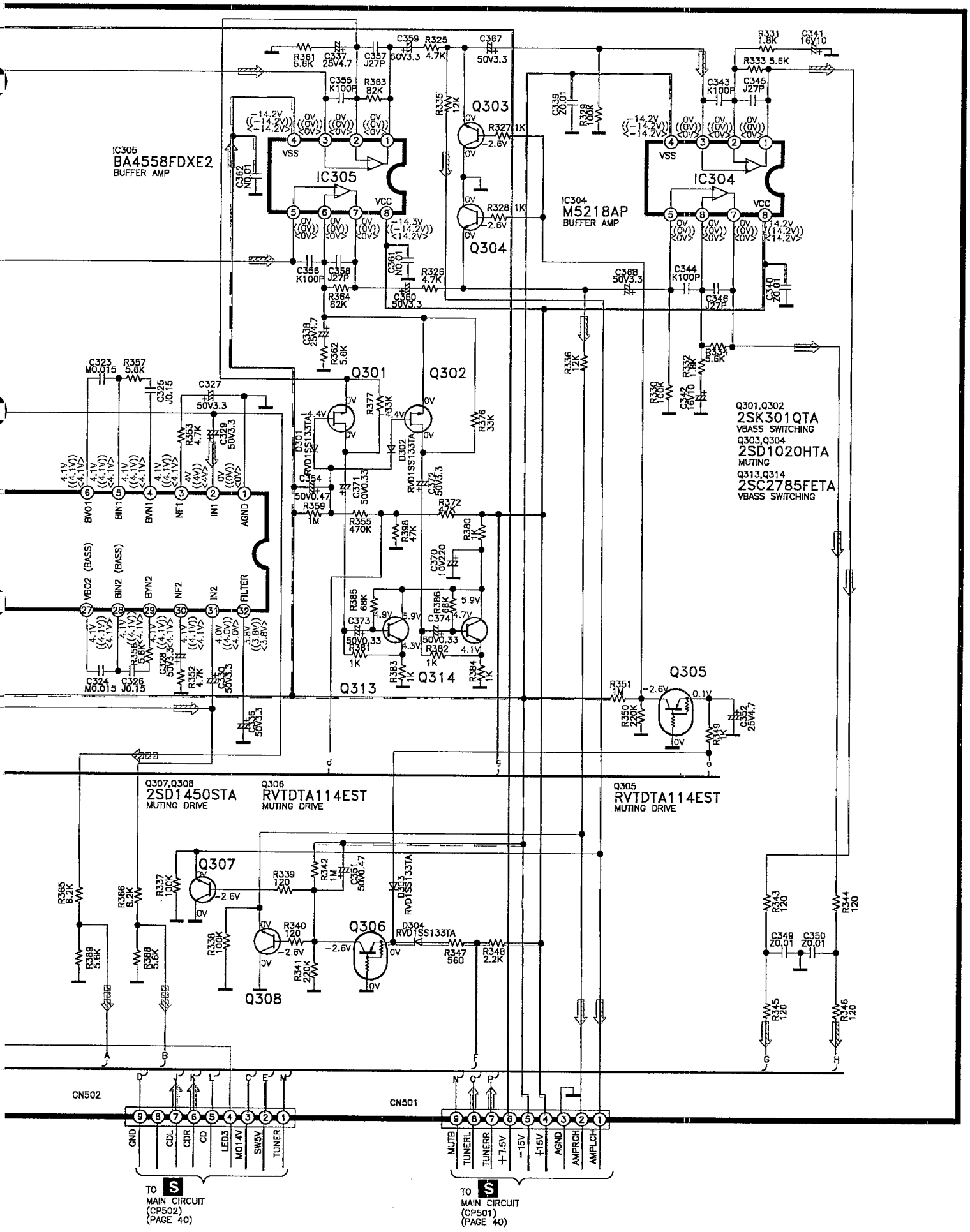




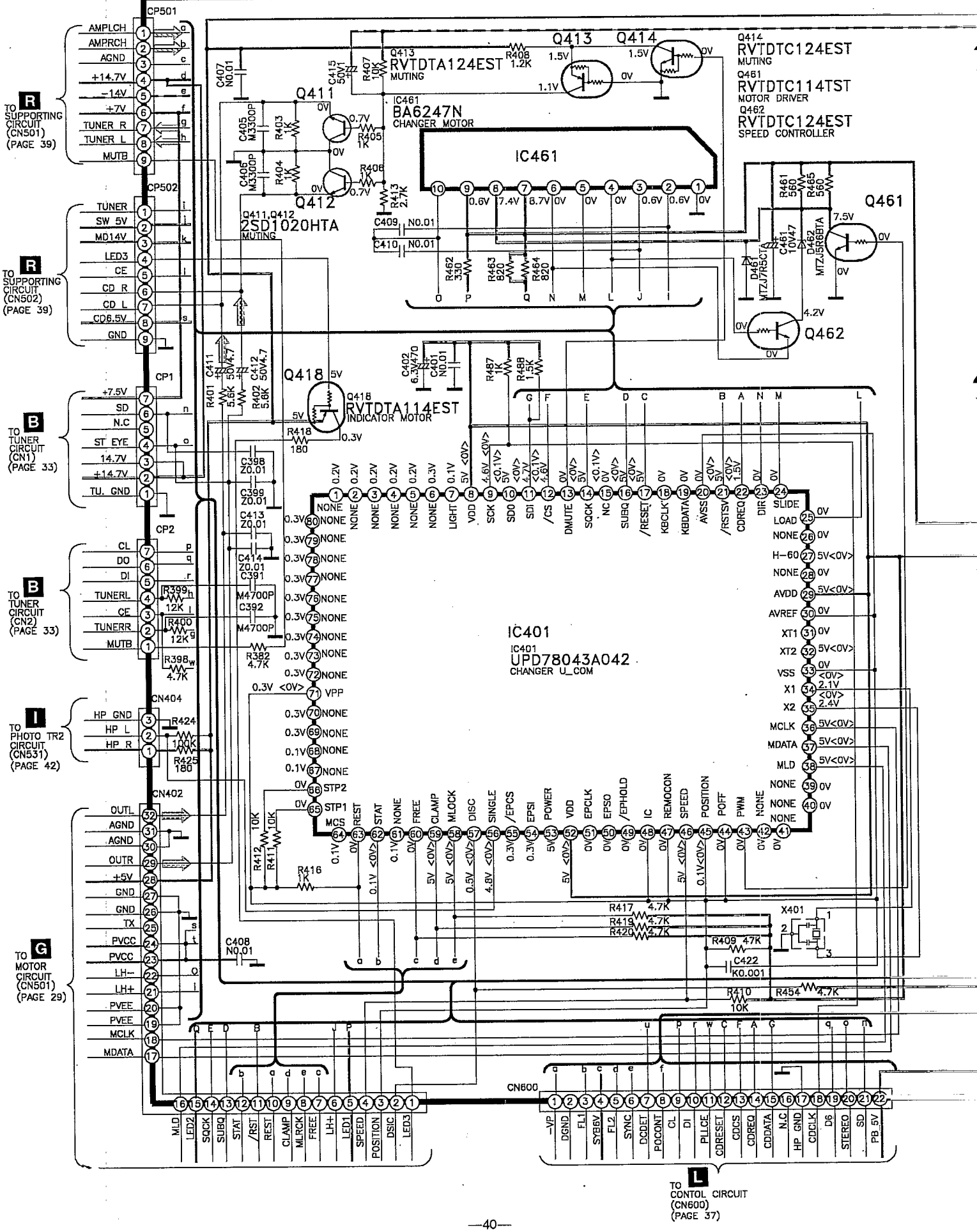
K HEADPHONE CIRCUIT

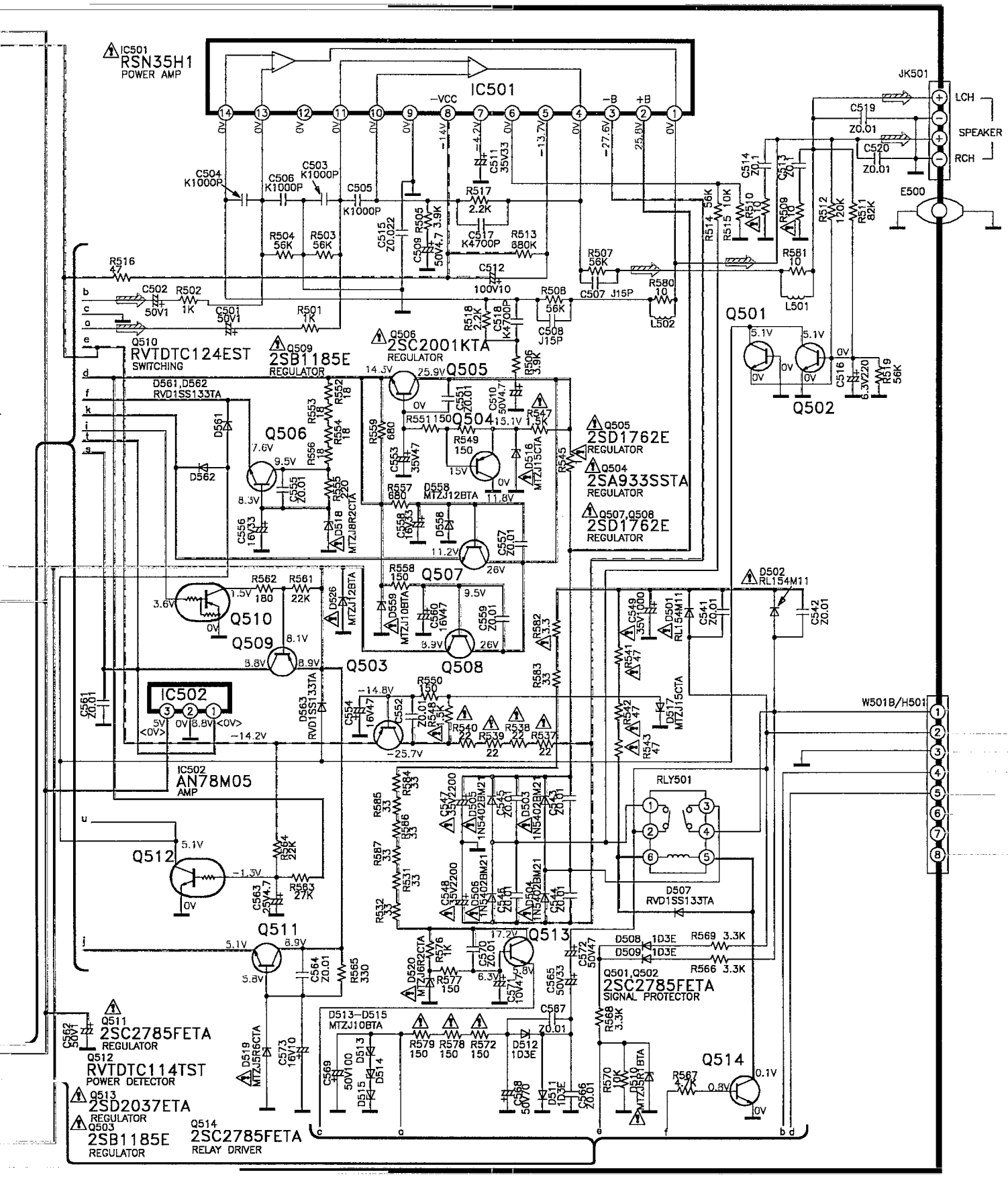
R SUPPORTING CIRCUIT



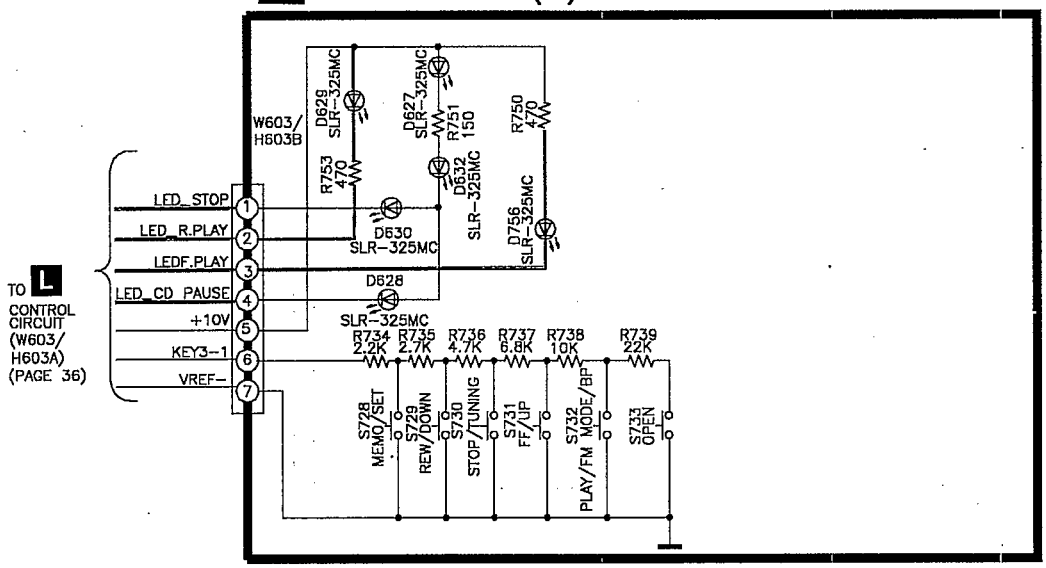

IC305
BA4558FDXE2
BUFFER AMP
IC304
M5218AP
BUFFER AMP
Q301,Q302
2SK301QTA
VBASS SWITCHING
Q303,Q304
2SD1020HTA
MUTING
Q313,Q314
2SC2785FETA
VBASS SWITCHING
Q307,Q308
2SD1450STA
MUTING DRIVE
Q306
RVTDTA114EST
MUTING DRIVE
Q305
RVTDTA114EST
MUTING DRIVE
CN502
CN501
GND
CDL
CDR
CD
LED3
MD14V
SW5V
TUNER
MUTB
TUNERL
TUNERR
+7.5V
−15V
+15V
AGND
AMPRCH
AMPLCH
TO S MAIN CIRCUIT (CP502) (PAGE 40)
TO S MAIN CIRCUIT (CP501) (PAGE 40)

S MAIN CIRCUIT

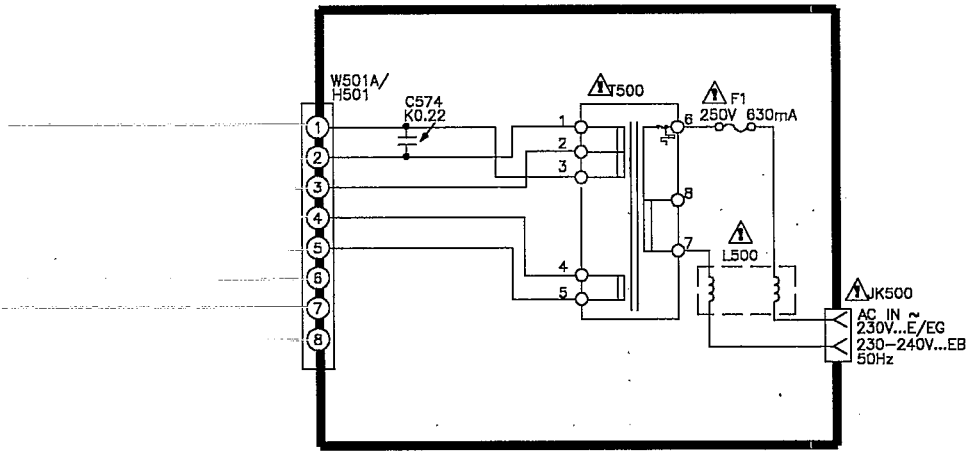



IC501
RSN35H1
POWER AMP
IC501
-VCC
-B
+B
JK501
LCH
SPEAKER
RCH
E500
Q501
Q502
L501
L502
Q510
RVTDTC124EST
SWITCHING
Q509
2SB1185E
REGULATOR
Q506
2SC2001KTA
REGULATOR
Q505
2SD1762E
REGULATOR
Q504
2SA933SSTA
REGULATOR
Q507,Q508
2SD1762E
REGULATOR
D561,D562
RVD1SS133TA
D502
RL154M11
W501B/H501
IC502
AN78M05
AMP
RLY501
D507
RVD1SS133TA
Q512
Q511
Q513
Q503
Q514
2SC2785FETA
REGULATOR
RVTDTC114TST
POWER DETECTOR
2SD2037ETA
REGULATOR
2SB1185E
REGULATOR
2SC2785FETA
RELAY DRIVER
Q501,Q502
2SC2785FETA
SIGNAL PROTECTOR
D513–D515
MTZJ10BTA

E OPERATION (2) CIRCUIT



J POWER CIRCUIT



I PHOTO TR2 CIRCUIT